REMARKS

At the outset, Applicant thanks the Examiner for examining the pending application. The Office Action dated October 29, 2007 has been received and its contents carefully reviewed.

Claims 1-15 are rejected. Applicant has amended claims 1, 4, 6-10 and 12-15 to further define the invention. No new matter has been added.

The Office Actions rejects claims 1-15 under 35 U.S.C. 103(a) as being unpatentable over Mizutome et al (6,037,920, hereinafter "Mizutome") in view of Mikami et al (6,727,875 B1, hereinafter "Mikami") and Takahashi et al (US 4,789,899, hereinafter "Takahashi").

Reexamination and reconsideration of the pending claims are respectfully requested.

Claim 1 is allowable over the cited references in that claim 1 recites a combination of elements including, for example, "a gate driving circuit for applying substantially identical first and second scan pulses to each one of the plurality of gate lines during one frame period of the LCD panel", "a data driving circuit for applying first and second data voltages having the same gray scale value to the data lines of the LCD panel in synchrony with the first and second scan pulses during the one frame period of the LCD panel, wherein the first and second scan pulses are applied at an interval in time each other during the one frame period of the LCD panel, and wherein the first and second data voltages are applied at an interval in time each other during the one frame period of the LCD panel".

Claim 10 is allowable over the cited references in that claim 10 recites a combination of elements including, for example, "applying first and second scan pulses to each of the plurality of gate lines during one frame period of the LCD panel, applying first and second data voltages having the same gray scale value to the plurality of data lines in synchrony with the first and second scan pulses during one frame period of the LCD panel, wherein the first and second scan pulses are applied at an interval in time each other during the one frame period of the LCD panel, and wherein the first and second data voltages are applied at an interval in time each other during the one frame period of the LCD panel".

Mikami (Figs. 7 and 8) discloses that one main pulse VGn is applied to specific scan wiring line 12 during one frame. At this time, a signal voltage Vd is selectively applied to four different pixels Pnx1 to Pnx4 in accordance with the sub scan pulses VGS1 and VGS 2 with four different combinations of H level and L level. Thus, Mikami does not teach that the main scan pulse VGn and the sub scan pulses VGS1 and VGS 2 have an interval in time during the one frame.

In addition, Mikami discloses that the signal voltage Vd one time is applied to the pixels Pnx1 to Pnx4 connected to the specific main scan wiring line during the one frame.

Therefore, Mikami does not disclose this feature of the claimed invention.

In the meantime, Takahashi (FIG. 2) discloses that two pulses p1 and p2 are applied to specific gate line during field scanning period. Image signal is applied to pixels connected to the specific gate line in accordance with the pulse p1 during a first half of the field scanning period, and a direct current potential VH is applied to pixels connected to the specific gate line in accordance with the pulse p2 during a second half of the field scanning period. Thus, in Takahashi, the image signal and the direct current potential VH having different voltages are applied to the pixels connected to the specific gate line. In contrast, first and second data voltages having the same gray scale value are applied to pixels connected to a specific gate line in the present invention.

Therefore, Mikami does not disclose this feature of the claimed invention.

As a result, none of the cited references, singly or in combination, teaches or suggests at least this feature of the claimed invention. Accordingly, Applicant respectfully submits that claims 1 and 10 and claims 2-9 and 11-15, which depend therefrom, are allowable over the cited references.

Applicant believes the application is in condition for allowance and early, favorable action is respectfully solicited. If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at (202) 496-7500 to discuss the steps necessary for placing the application in condition for allowance. All

correspondence should continue to be sent to the below-listed address. If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

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